

IN THE CLAIMS

Claims 1-17 (Canceled)

18. (Currently Amended) A semiconductor device including a MISFET, comprising:

- a semiconductor substrate having a first conduction type;

- a first semiconductor region having the first conduction type, formed in the semiconductor substrate;

- a second semiconductor region having a second conduction type which is opposite to the first conduction type, formed over the first semiconductor region;

- a third semiconductor region having the first conduction type, formed over the second semiconductor region;

- an insulating film formed over the third semiconductor region;

- a first hole reaching the second semiconductor region, formed in the third semiconductor region;

- a second hole connected to the first hole, formed in the insulating film; and

- a conductive film formed in the first and the second holes,

- wherein the conductive film is electrically connected to the second and the third semiconductor regions, and

a width of the second hole is larger than a width of the first hole,

the semiconductor substrate has a main surface and a back surface,

a trench reaching the first semiconductor region is formed in the main surface of the semiconductor substrate,

a gate insulating film of the MISFET is formed in the trench, and

a gate electrode of the MISFET is formed over the gate insulating film.

19. (Previously Presented) The semiconductor device according to claim 18, wherein:

the conductive layer in the second hole and the third semiconductor region are contacted at an upper surface and a side surface of the third semiconductor region.

20. (Canceled)

21. (Currently Amended) The semiconductor device according to claim ~~20~~ 18, wherein:

the first, the second, and the third semiconductor regions comprise a drain region, a channel-forming region, and a source region of the MISFET, respectively.

22. (Previously Presented) The semiconductor device according to claim 21, wherein:

the conductive layer in the second hole and the source region are contacted at an upper surface and a side surface of the source region.

23. (Canceled)

24. (New) A semiconductor device including a MISFET, comprising:

a first semiconductor region having a first conductive type and formed in a semiconductor substrate;

a second semiconductor region having a second conductive type opposite to said first conductive type and formed over said first semiconductor region;

a third semiconductor region having said first conductive type and formed over said second semiconductor region;

a first opening reaching said second semiconductor region and formed in said third semiconductor region such that said first opening exposes a side surface of said third semiconductor region;

a fourth semiconductor region of said second conductivity type formed in said second semiconductor region and formed in self-alignment with said first opening such that

an impurity concentration of said fourth semiconductor region is greater than that of said second semiconductor region and such that said first opening exposes said fourth semiconductor region; and

an insulating film formed over said third semiconductor region and having a second opening,

wherein said second opening has a width greater than that of said first opening such that said second opening exposes an upper surface of said third semiconductor region and said first opening, and

a conductive film is formed in said first opening and said second opening and electrically connected to said third semiconductor region and said fourth semiconductor region such that said conductive film is electrically connected to said upper surface of said third semiconductor region.

25. (New) A semiconductor device according to claim 24, further comprising:

a trench formed in said first semiconductor region, said second semiconductor region and third semiconductor region;

a gate insulating film of said MISFET formed on a side surface of said trench; and

a gate electrode of said MISFET formed on said gate insulating film such that said gate electrode is buried in said trench,

wherein said first semiconductor region serves as a drain region of said MISFET, and

wherein said third semiconductor region serves as a source region of said MISFET.

26. (New) A semiconductor device according to claim 25, wherein said fourth semiconductor region does not contact said trench.

27. (New) A semiconductor device including a MISFET, comprising:

a first semiconductor region having a first conductive type and formed in a semiconductor substrate;

a second semiconductor region having a second conductive type opposite to said first conductive type and formed over said first semiconductor region;

a third semiconductor region having said first conductive type and formed over said second semiconductor region;

a first opening reaching said second semiconductor region and formed in said third semiconductor region such that

said first opening exposes a side surface of said third semiconductor region;

a fourth semiconductor region of said second conductivity type formed in said second semiconductor region and formed in self-alignment with said first opening such that an impurity concentration of said fourth semiconductor region is greater than that of said second semiconductor region and such that said first opening exposes said fourth semiconductor region;

a conductive film formed in said first opening and electrically connected to said third semiconductor region and said fourth semiconductor region such that said conductive film is electrically connected to said upper surface of said third semiconductor region;

a trench formed in said first semiconductor region, said second semiconductor region and said third semiconductor region;

a gate insulating film of said MISFET formed on a side surface of said trench; and

a gate electrode of said MISFET formed on said gate insulating film such that said gate electrode is buried in said trench,

wherein said first semiconductor region serves as a drain region of said MISFET, and

wherein said third semiconductor region serves as a source region of said MISFET.

28. (New) A semiconductor device according to claim 27, wherein said fourth semiconductor region does not contact said trench.